COST-EFFECTIVE HIGH PERFORMANCE MONOLITHIC X-BAND LOW NOISE AMPLIFIERS

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ABSTRACT

A low cost and high performance X-band low-noise amplifier with ion-implanted MESFET technology has been demonstrated. Various design, material, and processing approaches have been evaluated in terms of yield, cost, and device performance. An average noise figure of 2.2 dB and standard deviation of 0.1 dB with an associated gain of 22.5 dB and standard deviation of 0.8 dB at center frequency band of 9.5 GHz has been measured.

INTRODUCTION

Recently, there has been a growing need for large quantities of inexpensive microwave and millimeter-wave monolithic components for active array radar applications. The major issue facing the use of active array antennas in radar system design is affordability. The affordability is further clouded by a lack of valid data from which performance and cost estimates can be made. In general, about 3,000 to 10,000 MMIC chips are needed to support a typical radar system. Therefore, a high rate GaAs MMIC chip fabrication must be developed to increase throughput and reduce the chip cost.

In this paper, we will describe a cost-effective technology to fabricate high performance GaAs X-band low noise amplifiers. The discussion includes design considerations, material approach, and processing technique which are essential to achieve our low cost, high performance objectives.

CIRCUIT DESIGN

The circuit design of the LNA has evolved as a result of both circuit refinements and new GaAs materials. To systematically improve the yield and performance, four design iterations have been carried out. A single FET geometry and the same basic circuit design were used for all four iterations. The first two versions were based on an existing FET fabricated by ion implantation into Cr-doped GaAs.[1] The first iteration LNA had 20 dB of gain and a 4 dB noise figure.[2] The second version flattened the gain response across the 9 to 10 GHz range while keeping the same noise figure. In order to improve the noise figure, the third and fourth versions were based on FETs using VPE and ion implantation into LEC substrates. These FETs had very similar characteristics, but were significantly different from the original FET fabricated on Cr-doped substrates. Between each iteration, we have comprehensively evaluated not only the FET devices but also the passive components in the monolithic circuits to determine the necessary layout modification. When the new S-parameters and equivalent noise model were incorporated, the final LNA design provided a circuit with a predicted 22 dB of gain and a 2.2 dB noise figure.

The final monolithic amplifier consists of two 0.5μm gate FETs with 300μm gate width, five 10 pF overlay capacitors, microstrip lines, and via holes to ground. The chip size is 1.9 x 2.0 mm as shown in Figure 1.

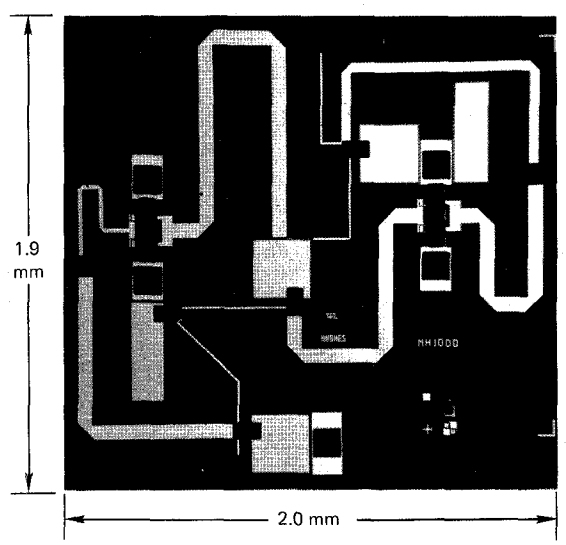

Figure 1 X-band 2 stage monolithic low noise amplifier.

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MMIC FABRICATION

A low cost, high yield process has been developed for the monolithic low noise amplifier fabrication.[3] A batch-wafer processing (typically six wafers per lot) is used to simulate a production condition and minimize the labor costs. The MMIC fabrication procedure includes formation of the FET channel layer, device isolation, fabrication of ohmic contacts, Schottky gates, overlay metallization for circuitry, MOM overlay capacitors, device passivation, airbridge interconnects, wafer thinning, via hole etching, and back metallization.

The key to fabricate the low cost, high yield, and high performance low noise MMICs is the use of ion implantation into qualified substrates. An important aspect of high yield GaAs FET fabrication is the utilization of high quality starting materials. Undoped LEC materials provide high quality and consistency. However, screening tests are still necessary to ensure good device yields and reproducibility. Substrate related effects and problems are defined and monitored by using standard process control monitoring techniques such as C-V profiles, I_{SAT} current, sheet resistivity, and FET characteristic measurements.

The gate fabrication is the most critical process determining the device performance and yield. An optical contact lithography process is used to produce high yield. An optical contact lithography process is used to produce high yield 0.5μm gates with higher throughput and more reliable equipment compared with a direct write E-beam process. With the former process, a throughput of over 10 wafers per hour with a yield of 80 percent or higher is achieved. Recess etch, metal deposition, and lift-off of gates are also crucial processes for good metal adhesion to the GaAs surface and low gate resistance for short gates. An electrical test pattern has been implemented to control and measure the yield and uniformity of gate length and alignment.

The fabrication of MOM overlay capacitors is another key yield-limiting area for MMIC circuits. There are five 10 pF MOM capacitors in the low noise amplifier. A small change in capacitor yield drastically changes the amplifier yield. For example, if the total yield excluding overlay capacitors is 40 percent, then the overall amplifier yield may be dropped down to 13 percent, if the yield of a single capacitor is only 80 percent. A typical MOM capacitor yield of 96 percent has been obtained using a 2000 Å sputtered SiO_2 film as dielectric. The other key processes such as airbridges and via holes typically provide high yields (>90 percent).

PERFORMANCE AND YIELD RESULTS

By using ion-implant and capless anneal techniques, good activation of the Si implant and abruptness of the doping profile were achieved. The peak concentration was about 2.6 to 2.9 x 10^{17} cm^{-3} with a penetration depth of 0.18μm. The final dc tests show excellent FET I_{DSS} uniformity for ion implanted channels. Table 1 shows some of the FET uniformity and yield information on nine recent wafers fabricated by the direct ion implantation process. The standard deviation of I_{DSS} is about 11 percent, demonstrating good channel thickness control, whereas the corresponding VPE uniformity is often greater than 20 percent. An extrinsic FET transconductance of 165 mS/mm has been achieved. More than 80 two-inch wafers have been processed with a best dc yield of 35 percent. With proper dc specification control, we can usually achieve over 80 percent RF yield of dc good chips. By increasing the data base and improving this dc-RF correlation, a basis for projecting amplifier RF functional yield on the basis of on-wafer dc yield can be developed.

TABLE 1
FET UNIFORMITY AND YIELD OF LOW-NOISE MONOLITHIC AMPLIFIERS

Lot No.	I_{DSS} of 600 μm FETs			DC Yield (%)
	Average (mA)	Standard Deviation (mA)	Uniformity (%)	
LNA-MH-584	96.3	10.0	10.4	35
LNA-MH-585	73.1	6.7	9.1	36
LNA-MH-586	107.5	9.2	8.5	41
LNA-MH-624	95.5	13.4	14.0	35
LNA-MH-625	61.1	7.1	11.8	43
LNA-MH-626	76 7	8.5	11.0	47
LNA-MH-672	75 6	9.1	12.0	47
LNA-MH-673	72.3	11.9	16.5	54
LNA-MH-674	68.2	7.2	10.6	49
AVERAGE	80.7	9.2	11.4	43

Performance of 18 low noise amplifier chips randomly selected from six wafers is illustrated in Figure 2. These six wafers were fabricated using the final version of the circuit design. The noise figure is measured without tuning and with a bias condition of V_D = 3.0 volts and I_D = 24 mA. The noise figure is less than 3.0 dB and the associated gain is more than 20 dB across the frequency band from 9 to 10 GHz. A best noise figure of 2.0 dB with an associated gain of 22 dB has been measured at 9.5 GHz. Histograms showing the mean values and standard deviations of noise figure and

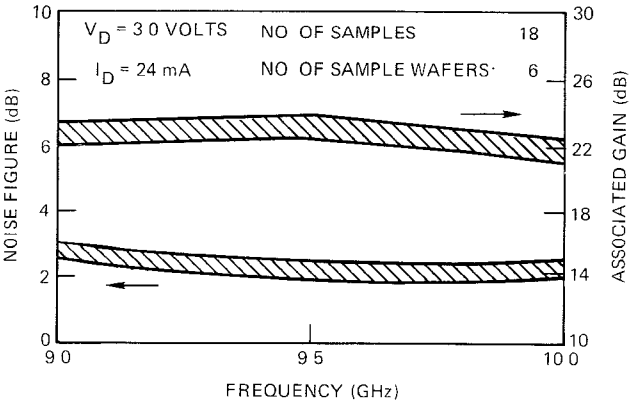

Figure 2 Frequency response of low noise amplifiers from recent 6 wafers with the final version design.

associated gain at 9.5 GHz are plotted in Figure 3. An average noise figure of 2.2 dB and standard deviation of 0.1 dB with an associated gain of 22.5 dB and standard deviation of 0.8 dB has been obtained from 18 samples. The noise figure and associated gain as functions of drain current are shown in Figure 4. It indicates that high gain with the same noise figure can be achieved at higher drain current between 24 and 42 mA.

COST REDUCTION TREND

The cost of GaAs monolithic IC chips will decrease as the technology matures and manufacturing throughput increases. Since the implanted LEC wafer has been adopted as the baseline material approach, we have gained the benefits of both yield and cost compared to VPE materials. Our recent data show that implanted wafers have at least a 10 percent higher device yield than VPE wafers because of better uniformity. Combining this yield factor and the lower cost of implanted materials, we can reduce the chip cost by a factor of two on X-band amplifiers. Through the process control monitoring and sensitivity analysis, it allows us to further improve yield by better controlling the process and designing a more tolerant circuit. In addition, ordinary silicon process techniques such as cassette handling, microprocessor control, and automated equipment must be implemented in GaAs processing. On this basis, we believe that an overall yield higher than 30 percent and a throughput greater than 100 wafers per week are realistic.

CONCLUSION

A high performance X-band monolithic low-noise amplifier with low cost ion implanted MESFET technology has been demonstrated. Through material/process uniformity improvement, process control monitor, and wafer handling improvements, we can further enhance the overall yield without degrading the projected high performance of the amplifier circuit. An extrinsic FET transconductance of 165 mS/mm and a best dc yield of 35 percent has been achieved. A typical noise figure of 2.0 to 2.4 dB with an associated gain of 20 to 23 dB has been measured at 9.5 GHz.

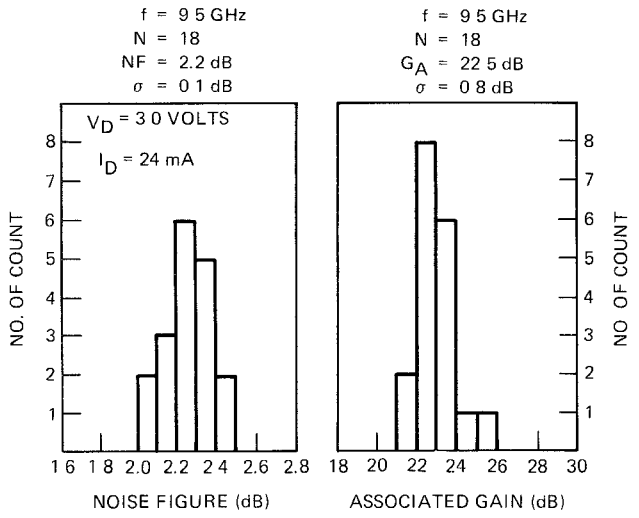

Figure 3 Historgram of noise figure and associated gain at 9.5 GHz.

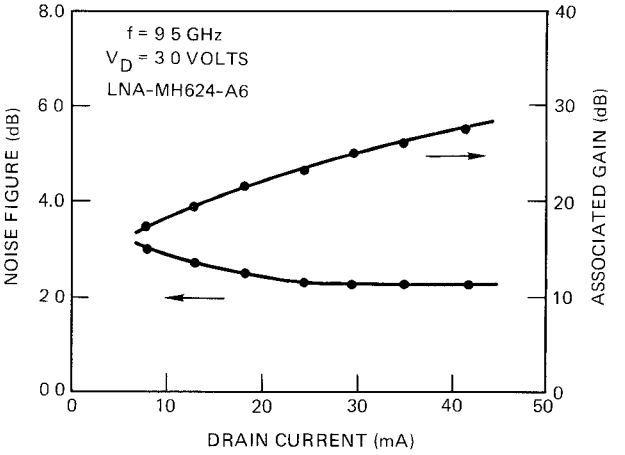

Figure 4 Noise figure and associated gain as functions of drain current.

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